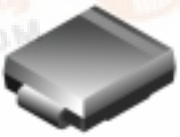
FAIRCHILD SEMICONDUCTOR TM

Discrete POWER & Signal Technologies

ES3A - ES3D

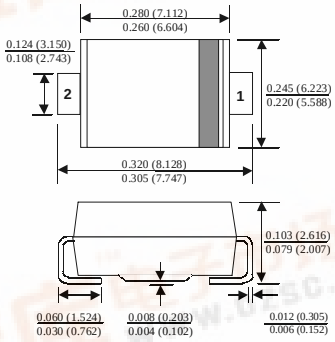
Features

- For surface mount applications.
- Glass passivated junction.
- Low profile package.
- Easy pick and place.
- Built-in strain relief.
- Superfast recovery times for high efficiency.



SMC/DO-214AB

COLOR BAND DENOTES CATHODE



3.0 Ampere Superfast Rectifiers

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
I_O	Average Rectified Current .375 " lead length @ T_A = 75°C	3.0	A
$i_{f(surge)}$	Peak Forward Surge Current 8.3 ms single half-sine-wave Superimposed on rated load (JEDEC method)	100	A
P_D	Total Device Dissipation Derate above 25°C	2.66 21.28	W mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient**	47	°C/W
$R_{\theta JL}$	Thermal Resistance, Junction to Lead**	12	°C/W
T_{stg}	Storage Temperature Range	-50 to +150	°C
T_J	Operating Junction Temperature	-50 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

**Device mounted on FR-4 PCB 0.013 mm.

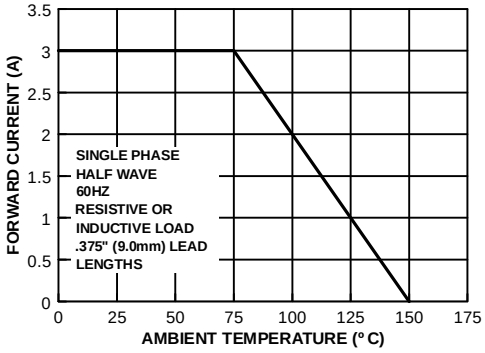
Electrical Characteristics

T_A = 25°C unless otherwise noted

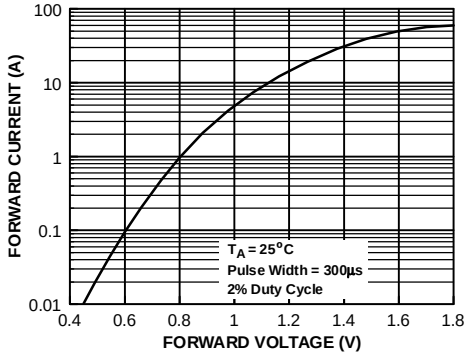
Parameter	Device				Units
	3A	3B	3C	3D	
Peak Repetitive Reverse Voltage	50	100	150	200	V
Maximum RMS Voltage	35	70	105	140	V
DC Reverse Voltage (Rated V_R)	50	100	150	200	V
Maximum Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	10 500				µA µA
Maximum Reverse Recovery Time I_F = 0.5 A, I_R = 1.0 A, I_{RR} = 0.25 A	20				nS
Maximum Forward Voltage @ 3.0 A	0.90				V
Typical Junction Capacitance V_R = 4.0 V, f = 1.0 MHz	45				pF

Typical Characteristics

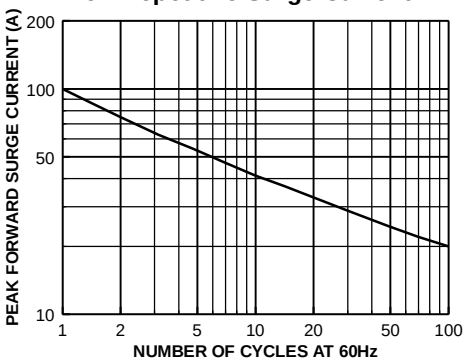
Forward Current Derating Curve



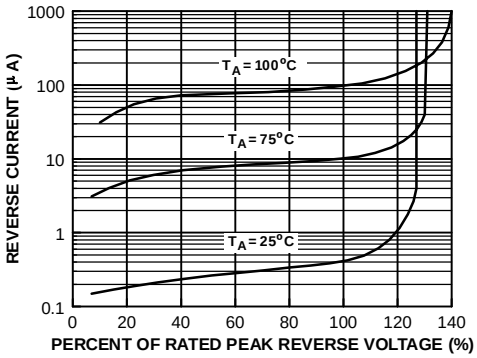
Forward Characteristics



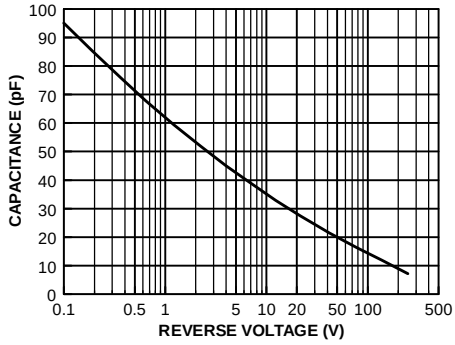
Non-Repetitive Surge Current

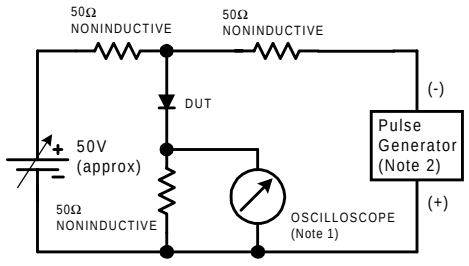


Reverse Characteristics

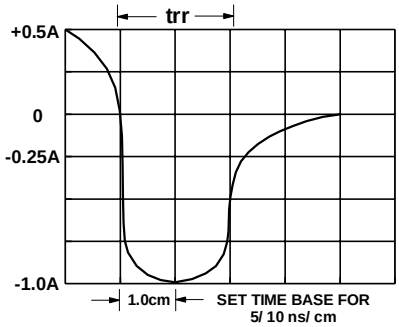


Junction Capacitance





NOTES:
1. Rise time = 7.0 ns max; Input impedance = 1.0 megaohm 22 pf.
2. Rise time = 10 ns max; Source impedance = 50 ohms.



Reverse Recovery Time Characterstic and Test Circuit Diagram

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